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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,324	LEE, JI YOUNG	
	Examiner	Art Unit	
	MARK MAIS	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 8-54, and 58-72 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. (USP 7,593,433).

3. With regard to claim 1, Wu et al. discloses a system for transferring a signal to a channel **[Abstract, channels are multiplexed into a single stream over a physical transport medium]**, comprising:

a storage unit **[Fig. 10, Scheduling table (ST) 1004]** *dedicated to* the channel **[Abstract, single stream channel; Fig. 10, output from FIFO buffer 1008 to channel 506, col. 13, lines 26-27]** for storing source identification information **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels**

comprising time/scheduling and Program Identifiers (PID) of the data to be transmitted, col. 14, lines 24-27] of a plurality of *predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** the source identification information *indicating* an order of priority of the plurality of *predetermined* sources for access to the channel **[Fig. 5B, scheduler & multiplexer 804 determines the order of the programs in which to transmit the (video) packets, col. 8, lines 32-34; Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8]**;

a plurality of selection circuits **[Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006]** for receiving input signals from *at least one of the plurality of predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** *and the source identification information of the plurality of predetermined sources from the storage unit* **[Fig. 10, CTRL 1002 receives program identification and program priority from ST 1004, col. 13, lines 15-19]**, each of the selection circuits selecting one of the plurality of input signals **[ST 1004 controls MUX 1006 in response to signals from CTRL 1002, col. 13, lines 9-10; MUX 1006 sends the selected data to channel 506 via FIFO 1008, col. 13, lines 23-27]**; and

a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel **[Fig. 10, filler packet inserter (FPI) 1012 and MUX 1006 are used, as necessary, to insert extra place holder packets for video programs (which are unable to**

maintain constant bit rate (CBR) on channel 506) in order to maintain a CBR, col. 13, lines 31-46].

4. With regard to claim 23, Wu et al. discloses a system for transferring a signals to channels **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7]**, comprising;

a plurality of storage units **[Fig. 10, Scheduling table (ST) 1004; plural tables, col. 13, lines 11-13; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple ST 1004s, as well]**, each storage unit being *dedicated to* one of the channels **[Abstract, single stream channel; Fig. 10, output from FIFO buffer 1008 to channel 506, col. 13, lines 26-27]**, and each storage unit being adapted to store source identification information **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of the data to be transmitted, col. 14, lines 24-27]** *indicating* an order of priority of *a plurality of predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** for access to the channel **[Fig. 5B, scheduler & multiplexer 804 determines the order of the programs in which to transmit the (video)**

packets, col. 8, lines 32-34; Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8];

for each of the plurality of channels **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7]**, a plurality of selection circuits **[Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple CTRL 1002/MUX 1006s, as well]** for receiving input signals from *at least one of* the *plurality of predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** *and the source identification information* **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of the data to be transmitted, col. 14, lines 24-27]** *of the plurality of predetermined sources from the plurality of storage units* **[Fig. 10, CTRL 1002 receives program identification and program priority from ST 1004, col. 13, lines 15-19]**, each of the selection circuits selecting one of the plurality of input signals in response to the source information **[ST 1004 controls MUX 1006 in response to signals from CTRL 1002,**

col. 13, lines 9-10; MUX 1006 sends the selected data to channel 506 via FIFO 1008, col. 13, lines 23-27]; and

for each of the plurality of channels [**Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7**], a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel [**Fig. 10, filler packet inserter (FPI) 1012 and MUX 1006 are used, as necessary, to insert extra place holder packets for video programs (which are unable to maintain constant bit rate (CBR) on channel 506) in order to maintain a CBR, col. 13, lines 31-46**].

5. With regard to claim 37, Wu et al. discloses a direct memory access (DMA) controller for controlling transfer of signals from *predetermined* input sources to output devices, a plurality of channels being connected to the output devices, the DMA controller [**Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7**] comprising:

a plurality of storage units [**Fig. 10, Scheduling table (ST) 1004; plural tables, col. 13, lines 11-13; Fig. 5A, note that a cable distribution system 550 includes multiple satellite**

channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple ST 1004s, as well], each storage unit being *dedicated to* one of the channels **[Abstract, single stream channel; Fig. 10, output from FIFO buffer 1008 to channel 506, col. 13, lines 26-27]**, and each storage unit being adapted to store source identification information **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of the data to be transmitted, col. 14, lines 24-27]** indicating an order of priority of the *predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** for access to the channel **[Fig. 5B, scheduler & multiplexer 804 determines the order of the programs in which to transmit the (video) packets, col. 8, lines 32-34; Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8]**;

for each of the plurality of channels **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7]**, a plurality of selection circuits **[Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col.**

7, lines 26-60; thus, also multiple CTRL 1002/MUX 1006s, as well] for receiving input signals from *at least one of* the *predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** *and the source identification information* **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of the data to be transmitted, col. 14, lines 24-27]** *of the predetermined sources from the plurality of storage units* **[Fig. 10, CTRL 1002 receives program identification and program priority from ST 1004, col. 13, lines 15-19; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of the data to be transmitted, col. 14, lines 24-27]**, each of the selection circuits selecting one of the plurality of input in response to source identification information **[ST 1004 controls MUX 1006 in response to signals from CTRL 1002, col. 13, lines 9-10; MUX 1006 sends the selected data to channel 506 via FIFO 1008, col. 13, lines 23-27]**; and

for each of the plurality of channels **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7]**, a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel **[Fig. 10, filler packet inserter (FPI) 1012 and MUX 1006 are used, as necessary,**

to insert extra place holder packets for video programs (which are unable to maintain constant bit rate (CBR) on channel 506) in order to maintain a CBR, col. 13, lines 31-46].

6. With regard to claim 51, Wu et al. discloses a method for transferring a signal to a channel **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Abstract, single stream channel; Fig. 10, output from FIFO buffer 1008 to channel 506, col. 13, lines 26-27; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7]**, comprising:

storing **[Fig. 10, Scheduling table (ST) 1004]** source identification information **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of the data to be transmitted, col. 14, lines 24-27]** for a plurality of *predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11]** the source identification information *indicating* an order of priority **[Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8]** of the plurality of *predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** for access to the channel **[Fig. 5B, scheduler & multiplexer 804 determines the order of the programs in which to transmit the (video) packets, col. 8, lines 32-34; Fig. 10,**

ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8];

providing a plurality of selection circuits **[Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple CTRL 1002/MUX 1006s, as well]** for receiving input signals from *at least one of* the *plurality of predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** *and the source identification information* **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of the data to be transmitted, col. 14, lines 24-27]** *of the plurality of predetermined sources* **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]**, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information **[ST 1004 controls MUX 1006 in response to signals from CTRL 1002, col. 13, lines 9-10; MUX 1006 sends the selected data to channel 506 via FIFO 1008, col. 13, lines 23-27]**;

with a checking circuit, checking outputs of the selection circuits and forwarding a selected input signal to the channel **[Fig. 10, filler packet inserter (FPI) 1012 and MUX 1006 are used, as necessary, to insert extra place holder packets for video programs (which are**

unable to maintain constant bit rate (CBR) on channel 506) in order to maintain a CBR, col. 13, lines 31-46].

7. With regard to claims 2 and 52, Wu et al. discloses that each selection circuit selects the selected input signal according to a state of a respective control input to the selection circuit **[Fig. 10, CTRL 1002 receives program identification and program priority from ST 1004, col. 13, lines 15-19]**.

8. With regard to claims 3 and 53, Wu et al. discloses that the storage unit is a register **[Fig. 10, ST 1004]**.

9. With regard to claims 4 and 54, Wu et al. discloses that the storage unit stores the source identification information **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of the data to be transmitted, col. 14, lines 24-27]** for the *plurality of predetermined* sources in order of priority of the ((*plurality of predetermined)*) sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** for access to the channel **[Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8]**.

10. With regard to claims 8 and 58, Wu et al. discloses that the circuit checks the outputs of the selection circuits in a predetermined sequence **[Fig. 10, filler packet inserter (FPI) 1012 and MUX 1006 are used, as necessary, to insert extra place holder packets for video programs (which are unable to maintain constant bit rate (CBR) on channel 506) in order to maintain a CBR, col. 13, lines 31-46; i.e., the video programs are continuously examined (predetermined sequence) to maintain the CBR; any possible sequence, col. 13, lines 27-31]**.

11. With regard to claims 9 and 59, Wu et al. discloses that the circuit sequentially checks the outputs of the selection circuits **[Fig. 10, filler packet inserter (FPI) 1012 and MUX 1006 are used, as necessary, to insert extra place holder packets for video programs (which are unable to maintain constant bit rate (CBR) on channel 506) in order to maintain a CBR, col. 13, lines 31-46; i.e., the video programs are continuously examined (sequentially) to maintain the CBR; any possible sequence, col. 13, lines 27-31]**.

12. With regard to claims 10 and 60, Wu et al. discloses that the sequence is determined by an order in which the source identification information **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of the data to be transmitted, col. 14, lines 24-27]** of the *plurality of predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** is stored in the storage unit **[Fig. 10, ST 1004 provides priority data indicating what programs have**

priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8].

13. With regard to claims 11 and 61, Wu et al. discloses that the circuit checks the outputs of the selection circuits in order of priority **[Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8]** of the *plurality of predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** for forwarding input signals to the channel **[Fig. 10, filler packet inserter (FPI) 1012 and MUX 1006 are used, as necessary, to insert extra place holder packets for video programs (which are unable to maintain constant bit rate (CBR) on channel 506) in order to maintain a CBR, col. 13, lines 31-46; i.e., the video programs are continuously examined (sequentially) to maintain the CBR (in priority order); any possible sequence, col. 13, lines 27-31]**.

14. With regard to claims 12 and 62, Wu et al. discloses that the system includes a plurality of channels **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7]**, input signals from the

plurality of predetermined sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** being able to be forwarded to the plurality of channels **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7]**.

15. With regard to claims 13 and 63, Wu et al. discloses a plurality of storage units **[Fig. 10, Scheduling table (ST) 1004; plural tables, col. 13, lines 11-13; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple ST 1004s, as well]** associated respectively with the plurality of channels **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7]**.

16. With regard to claims 14 and 64, Wu et al. discloses that each of the storage units **[Fig. 10, Scheduling table (ST) 1004; plural tables, col. 13, lines 11-13; Fig. 5A, note that a cable**

distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple ST 1004s, as well] stores source identification information **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of data to be transmitted, col. 14, lines 24-27]** for *a plurality of predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** that are able to forward input signals onto the channel associated with the storage unit **[Fig. 10, output from FIFO buffer 1008 to channel 506, col. 13, lines 26-27]**.

17. With regard to claims 15 and 65, Wu et al. discloses that the selection circuits are multiplexers **[Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple CTRL 1002/MUX 1006s, as well]**.

18. With regard to claims 16 and 66, Wu et al. discloses that the multiplexers **[Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple CTRL 1002/MUX 1006s, as well]** are ordered according to the sequence of the source identification

information **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of data to be transmitted, col. 14, lines 24-27]** stored in the storage unit **[Fig. 10, Scheduling table (ST) 1004; plural tables, col. 13, lines 11-13; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple ST 1004s, as well]**

19. With regard to claims 17 and 67, Wu et al. discloses that the multiplexers **[Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple CTRL 1002/MUX 1006s, as well]** are ordered according to priorities **[Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8]** of the *plurality of predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** for forwarding input signals to the channel **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7]**.

20. With regard to claims 18 and 68, Wu et al. discloses that the *plurality of predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** are applied to inputs of the selection circuits **[Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple CTRL 1002/MUX 1006s, as well]** according to a predetermined order **[Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8]**.

21. With regard to claims 19 and 69, Wu et al. discloses that the predetermined order depends on priority **[Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8]** of the *plurality of predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** for access to the channel **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the**

source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7].

22. With regard to claims 20 and 70, Wu et al. discloses that the source identification information **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of data to be transmitted, col. 14, lines 24-27]** is generated according to the predetermined order such that the selection circuits **[Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple CTRL 1002/MUX 1006s, as well]** select the *plurality of predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** based on priority **[Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8]** of the *plurality of predetermined* sources for access to the channel **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7**].

23. With regard to claims 21 and 71, Wu et al. discloses that a channel unit **[Fig. 5B, Statistical re-Multiplexer 503]** associated with the channel **[Fig. 5B, channel 506]** for processing information related to the channel.

24. With regard to claims 22 and 72, Wu et al. discloses that the storage unit **[Fig. 10, ST 1004]** is part of the channel unit **[Fig. 5B, Statistical re-Multiplexer 503]**.

25. With regard to claims 24 and 38, Wu et al. discloses that each selection circuit **[Fig. 10, Scheduling table (ST) 1004; plural tables, col. 13, lines 11-13; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple ST 1004s, as well]** selects the selected input signal according to a state of a respective control input to the selection circuit **[Fig. 10, CTRL 1002 receives program identification and program priority from ST 1004, col. 13, lines 15-19]**.

26. With regard to claims 25 and 39, Wu et al. discloses that one or more of the *(plurality of) predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** are allocated to one or more of the channels **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g.,**

multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7].

27. With regard to claims 26 and 40, Wu et al. discloses that the allocation of the (*plurality of) predetermined* sources [**Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67**] to the channels [**Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7**] is controllable by controlling storage of source identification information in the storage units [**ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of data to be transmitted, col. 14, lines 24-27**].

28. With regard to claims 27 and 41, Wu et al. discloses that the storage units are registers [**Fig. 10, ST 1004**].

29. With regard to claims 28 and 42, Wu et al. discloses that each of the storage units [**Fig. 10, ST 1004**] stores its source identification information [**ST 1004 identifies source streams or**

programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of data to be transmitted, col. 14, lines 24-27] for the (*plurality of) predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** in order of priority **[Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8]** of the (*plurality of) predetermined* sources for access to the associated channel **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7]**.

30. With regard to claims 29 and 43, Wu et al. discloses that the selection circuits are multiplexers **[Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple CTRL 1002/MUX 1006s, as well]**.

31. With regard to claims 30 and 44, Wu et al. discloses that the multiplexers **[Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006;**

Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple CTRL 1002/MUX 1006s, as well] are ordered according to the sequence of the source identification information **[ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of data to be transmitted, col. 14, lines 24-27]** stored in the storage unit **[Fig. 10, Scheduling table (ST) 1004; plural tables, col. 13, lines 11-13; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple ST 1004s, as well]**.

32. With regard to claims 31 and 45, Wu et al. discloses that the multiplexers **[Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple CTRL 1002/MUX 1006s, as well]** are ordered according to priorities **[Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8]** of the *(plurality of) predetermined* sources **[Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67]** for forwarding input signals to the channels **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g.,**

multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7].

33. With regard to claims 32 and 46, Wu et al. discloses that the (*plurality of) predetermined* sources [**Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67**] are applied to inputs of the selection circuits [**Fig. 10, interpreted as the combination of controller (CTRL) 1002 and multiplexer (MUX) 1006; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple CTRL 1002/MUX 1006s, as well**] according to a predetermined order [**Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8**].

34. With regard to claims 33 and 47, Wu et al. discloses that the predetermined order depends on priority [**Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8**] of the (*plurality of) predetermined* sources [**Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67**] for access to the channels [**Abstract, channels are multiplexed into a single stream over a physical transport**

medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7].

35. With regard to claims 34 and 48, Wu et al. discloses that the source identification information [**ST 1004 identifies source streams or programs, col. 13, lines 6-7; e.g., STs are used to schedule all data for all channels comprising time/scheduling and Program Identifiers (PID) of data to be transmitted, col. 14, lines 24-27**] is generated according to the predetermined order such that the selection circuits select the (*plurality of) predetermined* sources [**Fig. 5B, a plurality of video channels CH1 through CHn, col. 8, lines 9-11; Fig. 10, MUX 1006 receives the video programs through input signal lines 824a-n via FIFOs 1010a-n, col. 12, lines 66-67**] based on priority [**Fig. 10, ST 1004 provides priority data indicating what programs have priority and the amount of bandwidth at the transport channel 506 at each priority level, col. 13, lines 6-8**] of the (*plurality of) predetermined* sources for access to the channels [**Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7**].

36. With regard to claims 35 and 49, Wu et al. discloses a plurality of channel units **[Fig. 5B, Statistical re-Multiplexer 503; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple re-multiplexer 503s, as well]** associated respectively with the plurality of channels **[Abstract, channels are multiplexed into a single stream over a physical transport medium; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; e.g., Fig. 5C, ultimately, the source video channels (Fig. 5B, CH1 through CHn) are received by receivers 508(1-n)—which receive the entire bitstream, col. 9, lines 3-7]** for processing information related to the channels.

37. With regard to claims 36 and 50, Wu et al. discloses that each of the storage units **[Fig. 10, Scheduling table (ST) 1004; plural tables, col. 13, lines 11-13; Fig. 5A, note that a cable distribution system 550 includes multiple satellite channels 506 (e.g., multiple uplinks 552/downlinks 556), col. 7, lines 26-60; thus, also multiple ST 1004s, as well]** is part of one of the channel units **[Fig. 5B, Statistical re-Multiplexer 503]**.

Allowable Subject Matter

38. Claims 5-7 and 55-57 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims including the claim framework for allowing such claim limitation to be meaningful—for example, the following proposed claim drafted by the examiner and considered to distinguish patentably over the art of record in this application, is presented to applicant for consideration (for combination with claim 5):

Proposed claim: A system for transferring a signal to an output channel, comprising:

a plurality of storage registers connected to an output port of the output channel and dedicated to the output channel for storing source port identifiers of a plurality of predetermined sources determined by a network engineer;

the source port identifiers are transferred to each storage register and saved in one long bit sequence, wherein priority for access to the output channel is based on the respective bit locations of each source port identifier within the long bit sequence such that a complicated comparison operation is not required;

a plurality of selection circuits comprising

a plurality of multiplexers and

the plurality of storage registers,

wherein one selection circuit further comprises one group of multiplexers of the plurality of multiplexers, the one group of multiplexers are connected to one storage register of the plurality of storage registers,

wherein each multiplexer of the one group of multiplexers receives one source of the plurality of predetermined sources from one source port,

wherein each multiplexer of the one group of multiplexers performs a comparison of the source port identifier of the received source from one source port and the information from the storage register including the source port identifiers and the priority value associated with the source port identifiers, and selects the one source for output to the output channel only if the source port identifier associated with the one source has the highest priority within the long bit sequence; and

a circuit for checking outputs of the plurality of selection circuits and forwarding selected sources of the plurality of predetermined sources to the output channel.

Response to Arguments

39. Applicant's arguments with respect to claims 1-4, 8-54, and 58-72 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

40. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

41. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

42. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

(a) Wicki et al. (USP 5,892,766), Method and apparatus for coordinating access to an output of a routing device in a packet switching network

(b) Wu et al. (USP 7,016,337), System and method for multiple channel statistical re-multiplexing.

(c) Chen et al. (USP 6201793), Packet delay estimation in high speed packet switches.

(d) Steely, Jr. et al. (USP 6249520), High-performance non-blocking switch with multiple channel ordering constraints.

(e) Kawamura et al. (USP 7559031), Video display apparatus, video composition delivery apparatus, and system.

(f) Regev et al. (USP 6809944), CAM with automatic next free address pointer.

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK MAIS whose telephone number is (571)272-3138. The examiner can normally be reached on 5am-4pm.

44. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pankaj Kumar can be reached on 571-272-3011. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

45. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

September 9, 2009

/MARK MAIS/
Examiner, Art Unit 2467
/Pankaj Kumar/
Supervisory Patent Examiner, Art Unit 2467